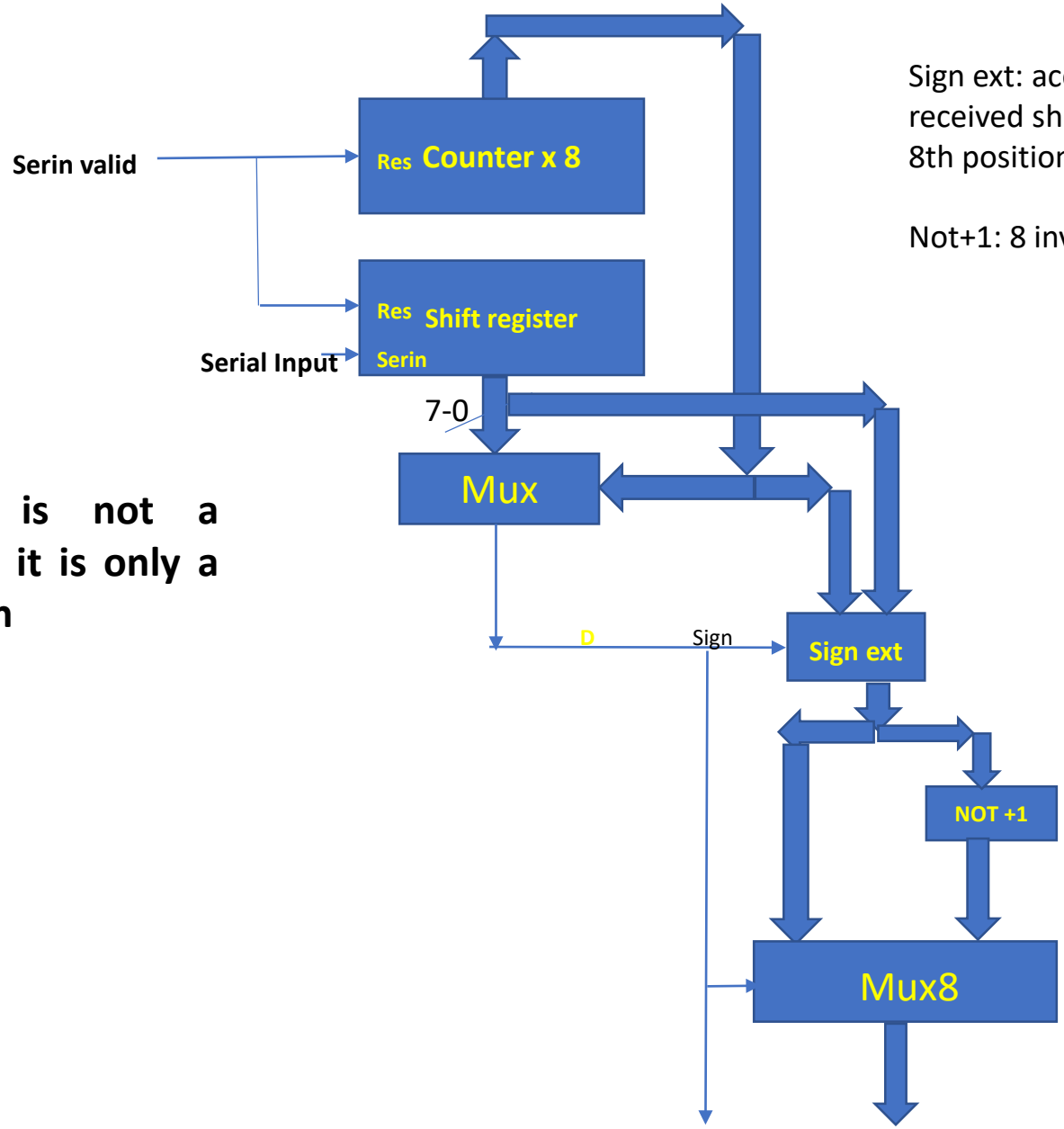
Digital Systems M

30-05-2017

With direct synthesis (using the usual blocks and combinatorial logical devices) and Vivado a synchronous system must be designed. The system is provided with the following signals:

- A serial input *Serin* where, starting from the least significant bit, 2's complement numbers are received with a variable number of bits (1 to 8).
- An input signal *Serin Valid* which is '1' during the reception of the serial input

The computed parallel data *(positive value)* and the sign must be stored in a parallel register



Sign ext: according to the value of the counter the last received shift register bit is extended (if needed) to the 8th position to fill the field up to the 8th position

Not+1: 8 inverters and a FA adding 1

Obviously this is not a *detailed* design: it is only a *conceptual* design

Result (positive value and sign to be sampled by Serin Valid!)