Exercise n. 1

Assume that a processor has a direct mapped cache. Data words are 8 bits long (i.e. 1 byte), data addresses are byte oriented, physical address is 20 bits long , the tag is 11 bits and each block holds 16 bytes of data. How many blocks are in this cache?

Since there are 20 bit for the address and the tag is 11 bit there are 9 bit left for the index and offset. Since each block holds 16 bytes, 4 bit of offset are needed. Therefore 5 bit are left for the indexing the cache. There are 2^5 or 32 blocks of 16 bytes in the cache (512 bytes)

Exercise n. 2

Consider a 16-way set-associative cache. Data words are 64 bits long, the cache holds 2 Mbytes of data, each way holds 16 data words of 64 bit. The physical address of the system is 64 bit.

1) How many ways in the entire cache?.
2) What is the number of sets of 16 ways?
3) What is the size of the tag of each way?

1) *Since the total size of the cache is 2MBytes (2^{21}) and each way is 16x8=128 bytes (2^7)there are $2^{21}/2^7 = 2^{14}$ = 16K ways*
2) *Since there are 16=2^4 ways for each set and in total 16Kways=2^{14} ways we have and $2^{14} / 2^4 = 2^{10}$ sets that is 1024 sets, each holding (128x4) bytes/way x 4 way/set= 2048 bytes*
1) *If the address is 64 bit, 7 bits are for addressing each byte in each way (128 bytes), 10 bit are used for the index (1024 sets) and therefore 64-7-10=47 bits are needed for each tag*

Exercise n. 3

Suppose you want modify the first stage of the pipelined DLX for introducing an interrupt mechanism which forces the system to execute instruction at address 0 when the interrupt flag is active. Suppose the interrupt flag is provided by a FF: how its reset must be activated in order to execute the interrupt routine only once for each activation. How can the return address can be granted.

Another input to the input mux of the first stage of the pipeline must be inserted forcing the pipeline to execute a branch (saving the return address in register 31) unconditionally to address zero. The interrupt flag must be automatically reset upon the insertion of forced jump into the pipeline and must be reenabled by a specific I/O command only after the return address is saved.