Computer architectures M
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1) Assume that for a given system with *40 bit virtual address* and *30 bit physical address* there is a TLB with 128 slots which provide the translation only of initial address of any page : the full physical address (to be presented to the cache) is therefore formed by joining the output of the TLB and the in-page address of the virtual address. If the page size is 8192 bytes how many entries (addresses) of the physical memory are covered by the TLB? And how many bits are present in the TLB?

2) The data forward mechanism in DLX is implemented by a sequential or combinatorial logical network? Describe the logic of the function which determines whether the forwarding mechanism must be activated.

3) Explain in detail the behaviour of the register renaming

1) The number of the is 128x8192 that is 1MB.

Each page (8192 bytes) requires 13 bit of addresses the number of bits is therefore

128 (slots) x [(40-13) + (30-13)] = 128 x 34 = 4352

input of the TLB output of the TLB

MSBits of the page initial virtual address MSBits of the page initial physical address

Forward (simplified)

Let's call X and Y the values of registers Ra and Rb extracted from the register file. The following *combinatorial* procedure applies separately for each of these registers.