Exercise 1

In a 4GB address space a 64 MB ram bank at addresses C0000000-C3FFFFFF must be implemented using 512 KB devices: how many devices are needed for implementing the bank? How many 64MB banks in a 4GB address space? What are the CS of the first and the last devices of the bank in a 8 bit parallelism environment? ? If the bank should be accessed by a processor with 32 bit parallelism what were the CS of the last 512 K of the bank?

Solution
In a 4 GB address space there are 64 banks of 64MB which means that the 6 most significant bits of the address determine the bank. [3FFFFFF is 3FF (1K) x FFFF (64K)]. Each bank uses therefore 26 of the 32 bit address for the internal addressing. To fill 64MB with 512KB devices 128 devices are needed. Since 512K => 0000-7FFFF (8x64K devices – do not forget zero address!) the last device must cover the addresses C3F80000-C3FFFFF while the first must cover the addresses C0000000-C007FFFF. With 8 parallelism the CS of the two 512K devices are therefore

(Lower addresses) CSL = A31 A30 A29! A28! A27! A26! A25! A24! A23! A22! A21! A20! A19!
(Upper addresses) CSU = A31 A30 A29! A28! A27! A26! A25 A24 A23 A22 A21 A20 A19

With a 32 bit parallelism the last 512 K of the bank should be implemented by 4x128K devices. The CS0 (CS1) (CS2) (CS3) would be therefore

CS0 (CS1) (CS2) (CS3) = A31 A30 A29! A28! A27! A26! A25 A24 A23 A22 A21 A20 A19 A18 A17 BE0 (BE1) (BE2) (BE3)

Exercise 2

What is behaviour of the register renaming within a reorder buffer?

Exercise 3

What are the characteristics of the link layer of the QPI in a full implementation? Indicate in detail all elements of the link and their meanings. What are the quadrants in QPI?

Notice: the exam papers should be easily READABLE which means that no *decryption* should be necessary for the correction, that page 2 follows page 1 etc *otherwise* I will not correct them with obvious consequences.