Exercise 1

a) In a 8 bit processor with 20 bit address a *single memory chip* of 64 KB must implement the processor addresses 32K-96K. What is its chip select expression ?

b) If the processor had a 16 bit parallelism and the same address system how could be the same memory space implemented with 32KB devices and what would be the CS?

Exercise 2

DLX processor has a 6 bit op-code field: is the number of different opcodes limited to 64? What is the maximum theoretical number of different opcodes if the opcode of instruction R format is fixed?

Exercise 3

A 16 bit address processor has a set-associative cache where the TAG is 10 bit and the line size in bit is 64 bit. If the cache associativity is 8 what is the size in bit of the cache if for each line two bit status are present and the cache has 8 slots?

Exercise 1

a) The address covered by the chip is 08000-17FFF. The CS expression must split into two parts as if the 64KB devices were made of two 32 KB portions:

08000-0FFFF 10000-17FFF

CS = AD19! AD18! AD17! AD16! AD15 + AD19! AD18! AD17! AD16 AD15!

b) Two 32KB devices. The same logic

CS0= AD19! AD18! AD17! AD16! AD15 BE0 + AD19! AD18! AD17! AD16 AD15! BE0

CS1= AD19! AD18! AD17! AD16! AD15 BE1 + AD19! AD18! AD17! AD16 AD15! BE1

Exercise 2

The answer is NO because the R instruction format has a 11 bit op-code extension which means that the number of different instructions is $63+2^{11} = 63+2048=2111$

Exercise 3

With 16 bit address and 10 bit tag, if there are 8 bytes/line there are 3 bit address for the line offset. The slot index value is made of three bits (16 address -10 tag -3 offset=3) For each slot there are 8 ways; each one of them is made of 10 bit tag, 64 bit datum and 2 status bit. The cache size is therefore

8 x [8x(10+64+2)]=4864 bit