1) Memory systems
2) DLX computer
3) IA basic architectures
4) Memory hierarchies and related problems of speed vs capacity.
5) Virtual memory memory concept, paging (one or more levels), TLB, inverted paging systems.
6) Cache architectures: full associative, directly mapped and set associative.
7) Cache coeherence problems. Single and multiprocessor MESI. Directory based coeherence.
8) Branch Target Address systems. Multilevel BTBs.
9) Replacement policies: hardware, counters, random.
10) Pipelines with multiple execution units, Scoreboarding, Tomasulo and ROB solutions. Register renaming.
11) P6 architecture
12) Pentium IV and its architecture. Centrino and Core 2.
13) Bus problems: parallel vs serial.
14) Quick Path Interconnections. Topologies and in depth ISO level analysis. MESIF.
15) QPI based microprocessors. Nehalem, Sandy Bridge, Haswell.

NB: the first three modules will be taught in order to grant to all students the same level of preparation and can be selectively skipped by the students who have already a good knowledge of the contents (which are however part of the official program of the course). The last four modules will be tentatively taught according to the time schedule of the course